Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Cancel).

2. (Currently Amended) ~~The~~ An image processing circuit ~~according to claim 1,~~ driven by a clock signal for processing data expressed by a plurality of bits, comprising:

a level determining section for determining whether or not a value of input data is smaller than a preset value; and

a clock control section for supplying a clock signal that makes a bit corresponding to the preset value active, when said level determining section determines that the value of the input data is not smaller than the preset value and interrupting supply of a clock signal that makes a bit corresponding to the preset value active, when said level determining section determines that the value of the input data is smaller than the preset value,

wherein said level determining section delays the result of determination by preset delay time from when values of successively input data items are changed from a value which is not smaller than the preset value to a value which is smaller than the preset value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the preset value to the value which is smaller than the preset value.

3. (Original) The image processing circuit according to claim 2, wherein the delay time is image processing time from when data is input to the image processing circuit until the data is output therefrom.

Claims 4 – 7 (Cancel).

8. (Currently Amended) ~~The~~ An image processing apparatus ~~according to claim 7,~~ including an image processing circuit driven by a clock signal for processing image data expressed by a plurality of bits, comprising:

a level determining section for determining whether or not a density value of image data input to the image processing circuit is smaller than a preset density value; and

a clock control section for supplying a clock signal that makes a bit corresponding to the preset density value active, when said level determining section determines that the density value of the input image data is not smaller than the preset density value and interrupting supply of a clock signal that makes a bit corresponding to the preset density value active, when said level determining section determines that the density value of the input image data is smaller than the preset density value,

wherein said level determining section delays the result of determination by preset delay time from when density values of successively input image data items are changed from a value which is not smaller than the preset density value to a value which is smaller than the preset density value until the preset delay time has elapsed in a case where the density values of the successively input image data items are changed from the value which is not smaller than the preset density value to the value which is smaller than the preset density value.

Claims 9 – 12 (Cancel).

13. (Currently Amended) ~~The~~ A control method ~~for the image processing circuit according to claim 12,~~ for controlling an image processing circuit driven by a clock signal for processing data expressed by a plurality of bits, comprising:

a first step of determining whether or not a value of input data is smaller than a preset value; and

a second step of supplying a clock signal that makes a bit corresponding to the preset value active, when it is determined in said first step that the value of the input data is not smaller than the preset value and interrupting supply of a clock signal that make a bit corresponding to the preset value active, when it is determined in said first step that the value of the input data is smaller than the preset value,

wherein said first step includes a step of delaying the result of determination by preset delay time from when values of successively input data items are changed from a value which is not smaller than the preset value to a value which is smaller than the preset value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the preset value to the value which is smaller than the preset value.

Claims 14 – 16 (Cancel).